This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

Claims 1-18 cancelled.

19. (currently amended) A method of fabricating multiple layers of a memory device, comprising:

assembling a common substrate having multiple sections;

constructing at least one fold line on the substrate to separate the multiple sections;

fabricating memory structure on at least two sections of the substrate;

depositing a semiconductor layer on at least one section of the substrate; and

folding the substrate along the fold line to stack the multiple sections on top of each other and align the memory structures on adjacent folded sections so that the memory structures interact with each other to thereby form ~~at least one operable electrical device~~a plurality of diodes.

20. (original) The method of fabricating multiple layers of a memory device recited in claim 19, wherein the method comprises assembling a substrate having a fold line to form two sections.

21. (original) The method of fabricating multiple layers of a memory device recited in claim 19, wherein the memory structure on at least one section further comprises fabricating diode fuse patterns on at least one of the two sections, and aligning the two sections so that the diode fuse patterns coincide to form a matrix of diode fuses.

22. (original) The method of fabricating multiple layers of a memory device recited in claim 20 wherein the memory structure on the two sections are fabricated to include conductor grids, the grids on the first section being perpendicular to the grids on the second section.

23. (original) The method of fabricating multiple layers of a memory device recited in claim 22, wherein the conductor grids of at least one of the first and second sections include conductors that vary in cross-section area at selected points on the conductors.

24. (original) The method of fabricating multiple layers of a memory device recited in claim 19, wherein the fold line is fabricated by applying multiple aligned perforations.

25. (original) The method of fabricating multiple layers of a memory device recited in claim 19, wherein at least two fold lines are fabricated on the substrate to provide at least three separate sections capable of folding to a stacked layer configuration.

26. (original) The method of fabricating multiple layers of a memory device recited in claim 25, wherein the sections are folded so that a center section on the substrate becomes a center layer of the folded sections.

27. (original) The method of fabricating multiple layers of a memory device recited in claim 25, wherein the sections are folded so that one of the end sections on the substrate becomes a center layer of the folded sections.

28. (original) The method of fabricating multiple layers of a memory device recited in Claim 25 wherein the at least two fold lines are parallel with each other.

29. (original) The method of fabricating multiple layers of a memory device recited in Claim 25 wherein the at least two fold lines are not parallel with each other.

30. (previously presented) A method of fabricating multiple layers of a memory device, comprising:

assembling a common substrate having multiple sections;

constructing at least one fold line on the substrate to separate the multiple sections;

fabricating memory structure on at least two sections of the substrate; and

folding the substrate along the fold line to stack the multiple sections on top of each other and align the memory structures on adjacent folded sections to form at least one operable electrical device, wherein the memory structure on at least one section further comprises fabricating diode fuse patterns on at least one of the two sections, and aligning the two sections so that the diode fuse patterns coincide to form a matrix of diode fuses.